

Appl. No. 10/603,570  
Amdt. Dated July 12, 2006  
Reply to Office Action of April 12, 2006

Attorney Docket No. 81707.0186  
Customer No.: 26021

REMARKS/ARGUMENTS:

Claims 2 and 3 are canceled without prejudice. Claims 1, 9, and 10 are amended. Claims 1 and 4-12 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

The present invention relates to a thermoelectric module having excellent thermoelectric characteristics that can be used for cooling heat-generating members such as semiconductors and optical integrated circuits, and to a process for producing the same. (Applicant's specification, at p. 1, lines 6-10).

CLAIM OBJECTIONS:

Claim 9 stands objected to because in line 10, the word "the" appears to be a typo. In response, the Applicant changed "the" to --a--. Withdrawal of this objection is thus respectfully requested.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102:

Claims 1-3, 7, and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Cauchy et al. (U.S. Patent No. 6,103,967). This rejection is moot with respect to claims 2 and 3 due to the cancellation of these claims. The Applicant respectfully traverses the rejection as to amended claim 1. Claim 1, as amended, is as follows.

A thermoelectric module comprising support substrates, a plurality of wiring conductors formed on the opposing surfaces of the support substrates, a plurality of thermoelectric elements, and solder layers formed between said wiring conductors and said thermoelectric elements, wherein the total projected area ( $S_v$ ) of voids contained in said solder layers projected onto the surfaces of the support substrates

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on the side where the solder layers are in contact via the wiring conductors is from 1 to 20% of the total area ( $S_t$ ) of the surfaces on where the solder layers are in contact with the wiring conductors, wherein said thermoelectric elements are provided with plated layers on the surfaces in contact with the solder layers, wherein said plated layers are formed by plating with nickel and gold.

Applicant respectfully submits that Cauchy cannot anticipate or render obvious amended claim 1, because Cauchy fails to teach or suggest that the plated layers are formed by plating with nickel and gold.

It is an aspect of the present invention that upon forming Au-plated layers 7b on the nickel-plated layers 7a, enhanced wettability is exhibited to the solder paste and, as a result, junction strength to the solder layers 6 and reliability are easily improved. It is desired that the Au-plated layers 7b have a thickness of 0.01 to 10  $\mu\text{m}$  by taking into consideration the cost of the material and a drop in the workability due to the ductility of Au in addition to wettability. (Applicant's specification, at p. 16, lines 6-13).

In contrast, the metallized layers of Cauchy are typically made of nickel and can contain a small percentage of phosphorous or boron. (Cauchy, column 3, lines 15-26). Cauchy fails to teach or suggest the use of a gold metallized layer either alone or together with the nickel metallized layer.

In light of the foregoing, Applicant respectfully submits that Cauchy could not have anticipated or rendered obvious claim 1, because Cauchy fails to teach or suggest each and every claim limitation. Claims 7 and 8 depend from claim 1 and cannot be anticipated or rendered obvious for at least the same reasons as claim 1. Withdrawal of these rejections is thus respectfully requested.

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CLAIM REJECTIONS UNDER 35 U.S.C. §103:

Claims 4-6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cauchy as applied to claims 1-3, 7, and 8 above, and further in view of Zhu (Thermal Impact of Solder Voids in the Electronic Packaging of Power Devices, 15<sup>th</sup> IEEE SEMI-THERM Symposium, 1999, pgs 22-29) and Lau et al. (Effects of Voids on Bump Chip Carrier (BCC++) Solder Joint Reliability, 2002 Electronic Components and Technology Conference, May 28-31 2002, pgs 992-1000). The Applicant respectfully traverses this rejection.

Claims 4-6 depend from claim 1 and therefore, cannot be rendered obvious over Cauchy for at least the same reasons discussed above. Zhu cannot remedy the defect of Cauchy and is not relied upon by the Office for such. Instead, the Office cites Zhu for teaching an average thickness for the solder layer of 50  $\mu\text{m}$ ; and for teaching void percentages less than 20% maintain extremely low variations in thermal transmission through the solder and distributed shallow voids, produce the lowest amount of thermal variations. Lau, similarly, cannot remedy the defect of Cauchy and is not relied upon by the Office for such. Instead, the Office cites Lau for teaching void sizes of 25, 50, and 75  $\mu\text{m}$  and showing the effect these sizes have on crack formation within the solder layer. Neither Zhu nor Lau teach or suggest the use of a gold metallized layer either alone or together with a nickel metallized layer.

In light of the foregoing, Applicant respectfully submits that the cited references could not have rendered claims 4-6 obvious, because the cited references fail to teach or suggest each and every claim limitation. Withdrawal of this rejection is thus respectfully requested.

Claims 9-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cauchy in view of Lau and Jafri (U.S. Patent No. 4,895,606). The Applicant

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respectfully traverses this rejection as to amended claim 9. Claim 9, as amended, is as follows:

A process for producing a thermoelectric module having at least support substrates, a plurality of wiring conductors formed on the opposing surfaces of the support substrates and a plurality of thermoelectric elements, by applying a solder paste containing a void-forming agent onto the surfaces of either the wiring conductors or the thermoelectric elements in the thermoelectric module, and joining said wiring conductors and said thermoelectric elements together by a heat treatment, wherein said thermoelectric elements are provided with plated layers on the surfaces in contact with the solder paste, wherein said plated layers are formed by plating with nickel and gold.

Claim 9, as amended, requires that the plated layers are formed by plating with nickel and gold. Consequently, claim 9 is patentable over Cauchy and Lau for the reasons discussed above. Jafri cannot remedy the defect of Cauchy and Lau and is not relied upon by the Office for such. Instead, the Office cites Jafri for teaching formulations for soldering flux. Jafri fails to teach or suggest the use of a gold metallized layer either alone or together with a nickel metallized layer.

In light of the foregoing, Applicant respectfully submits that the cited references could not have rendered claim 9 obvious, because the cited references fail to teach or suggest each and every claim limitation. Claims 10-12 depend from claim 9 and cannot be rendered obvious for at least the same reasons as claim 9. Withdrawal of these rejections is thus respectfully requested.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

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If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Date: July 12, 2006

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